FIG.1 PRIOR ART

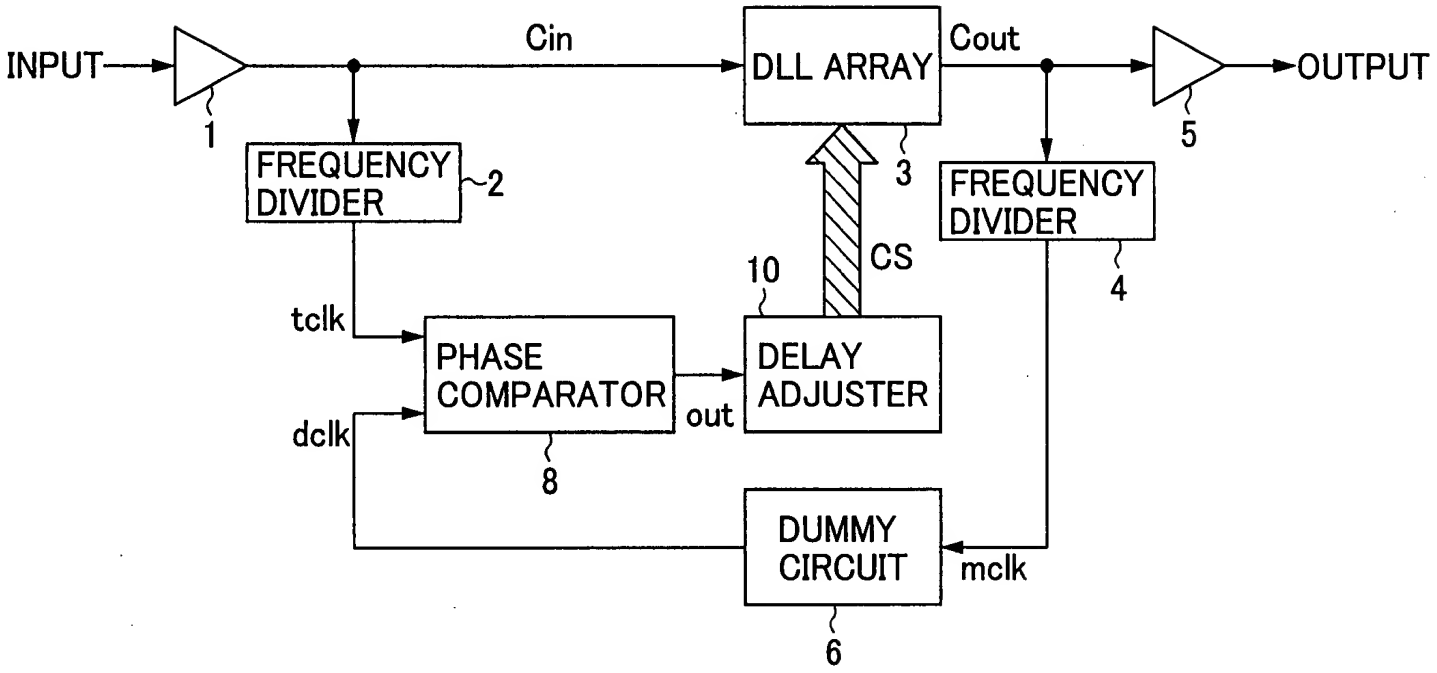

FIG. 2 PRIOR ART

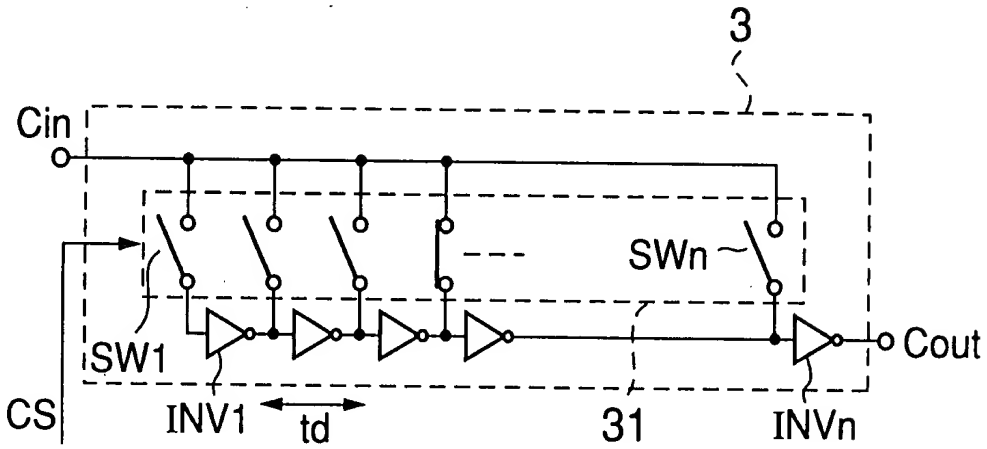

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FIG. 3
PRIOR
ART

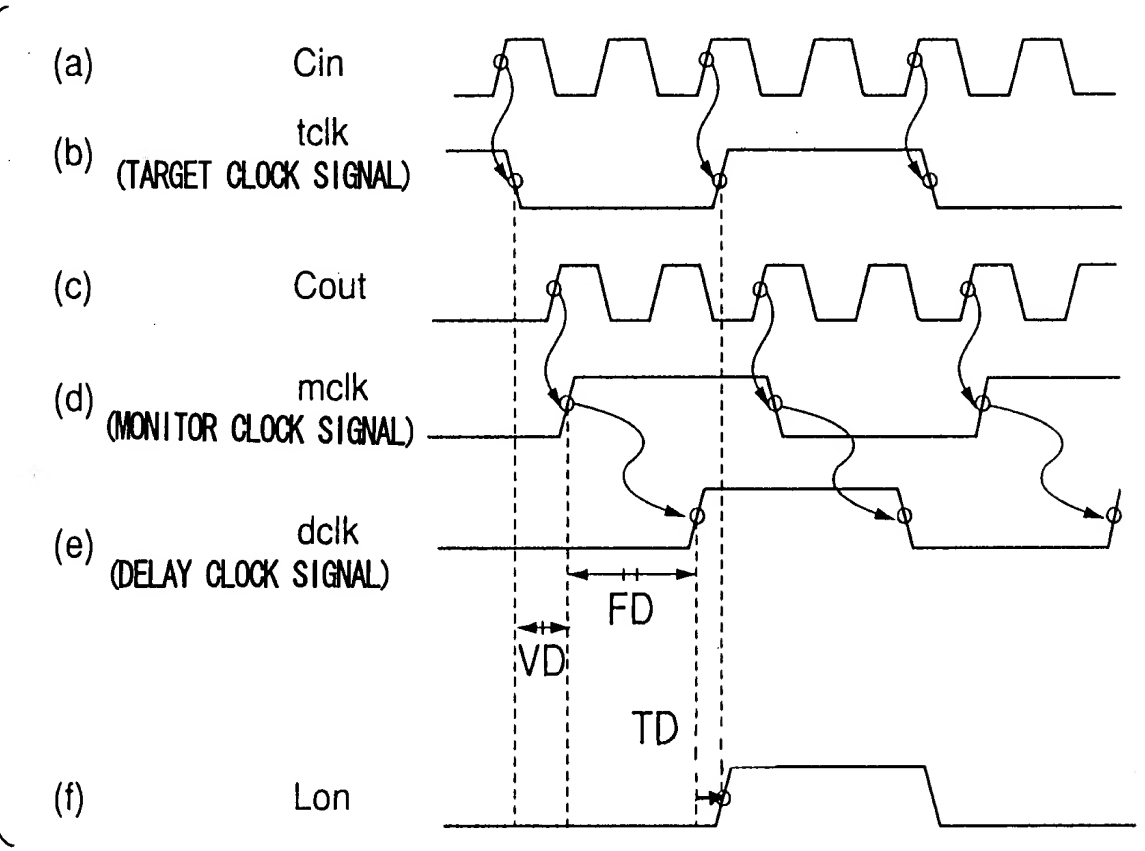


FIG. 4
PRIOR
ART

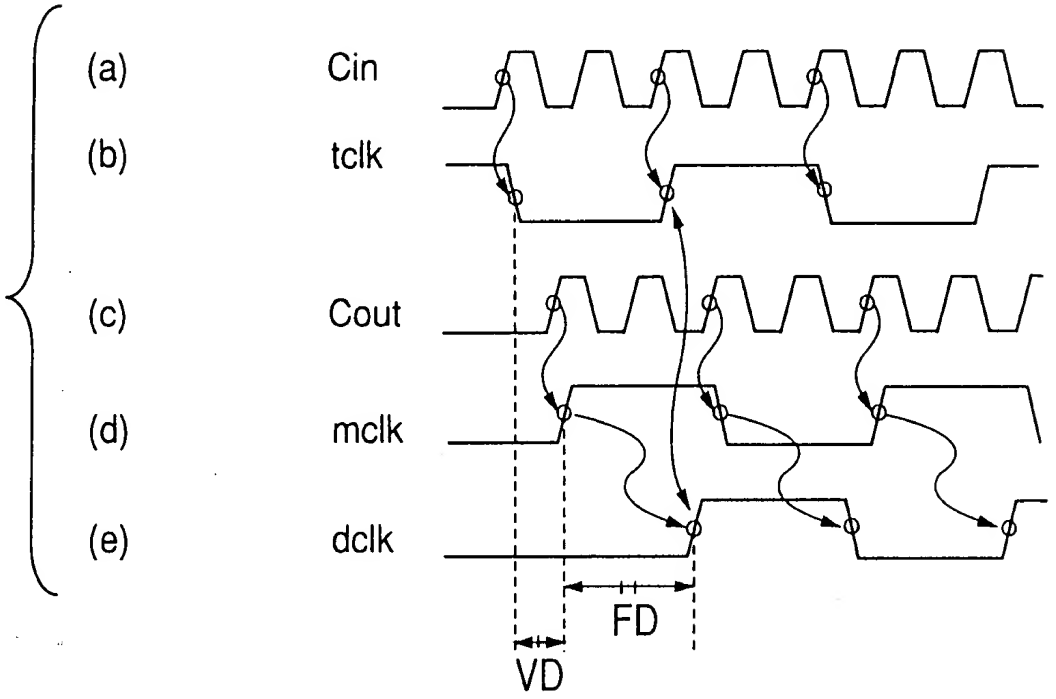


FIG.5

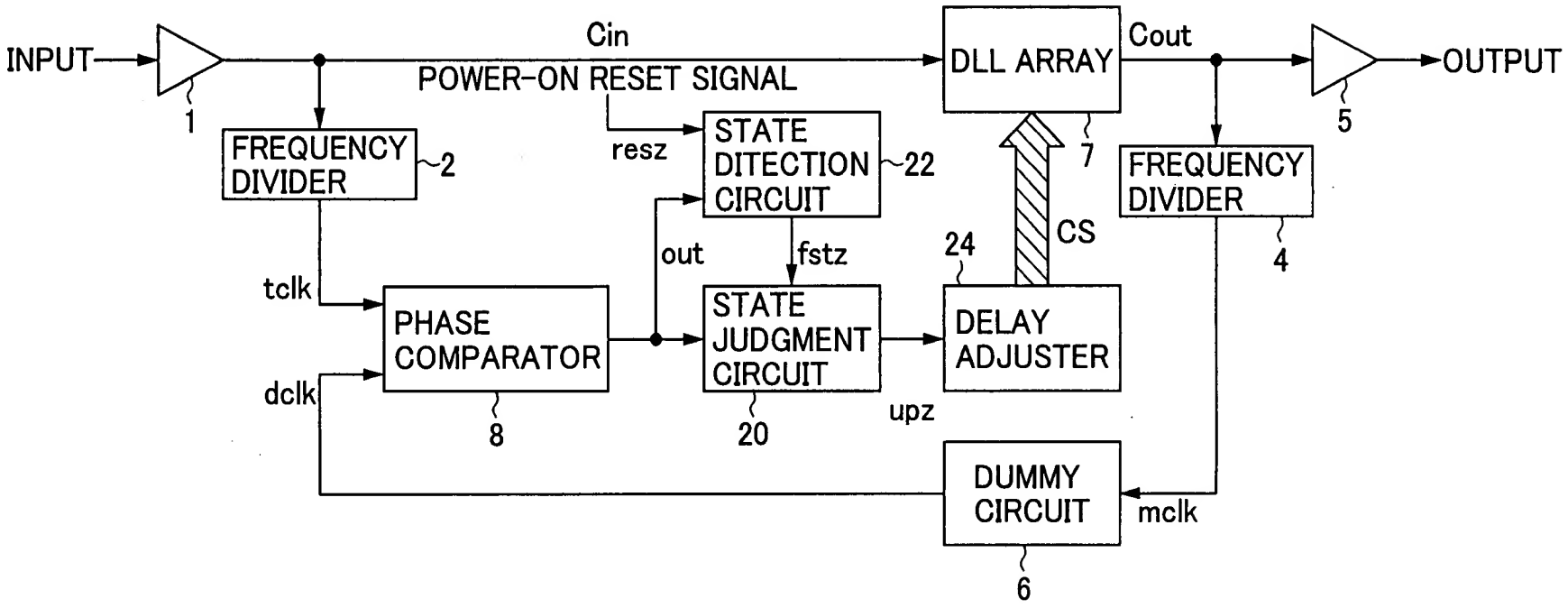
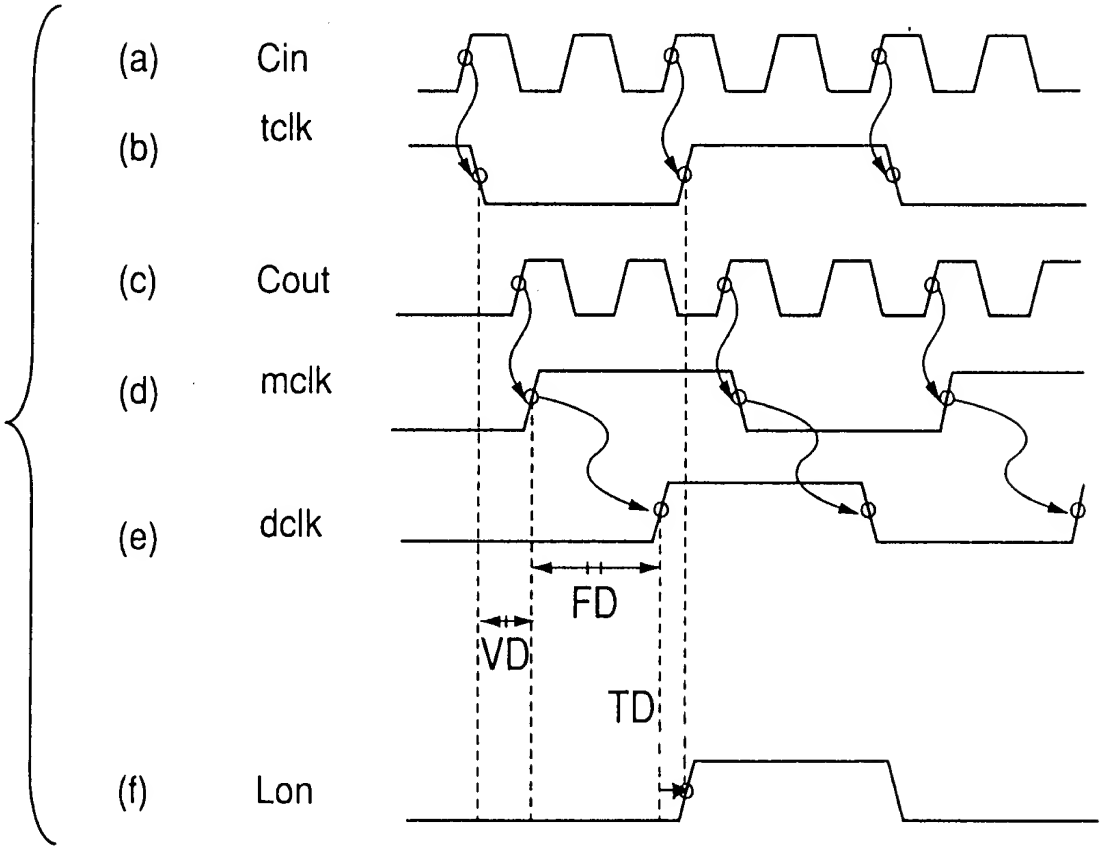

INPUT
1
Cin
POWER-ON RESET SIGNAL
DLL ARRAY
Cout
OUTPUT
5
FREQUENCY DIVIDER
2
resz
STATE DITECTION CIRCUIT
22
7
FREQUENCY DIVIDER
4
CS
24
out
fstz
tclk
PHASE COMPARATOR
8
STATE JUDGMENT CIRCUIT
20
upz
DELAY ADJUSTER
dclk
DUMMY CIRCUIT
6
mclk

FIG. 6



09727697 020020

FIG. 7

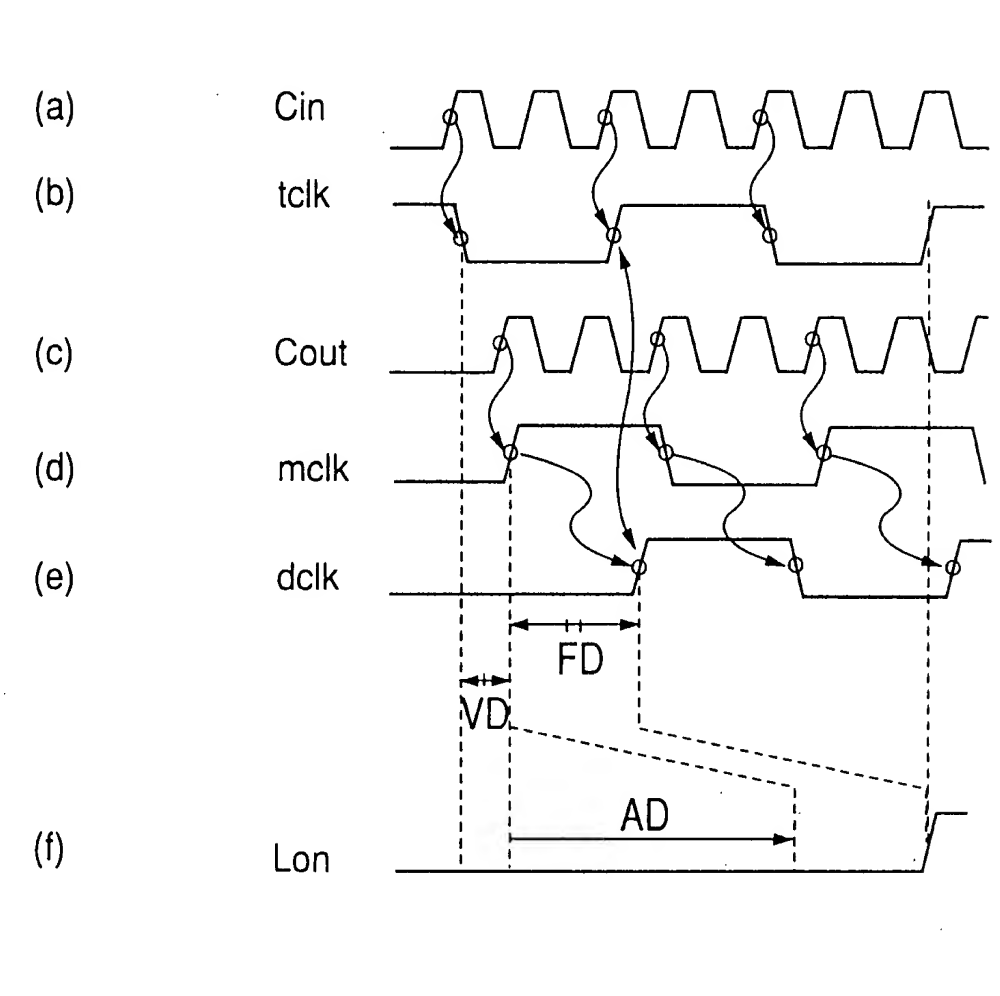


FIG. 8

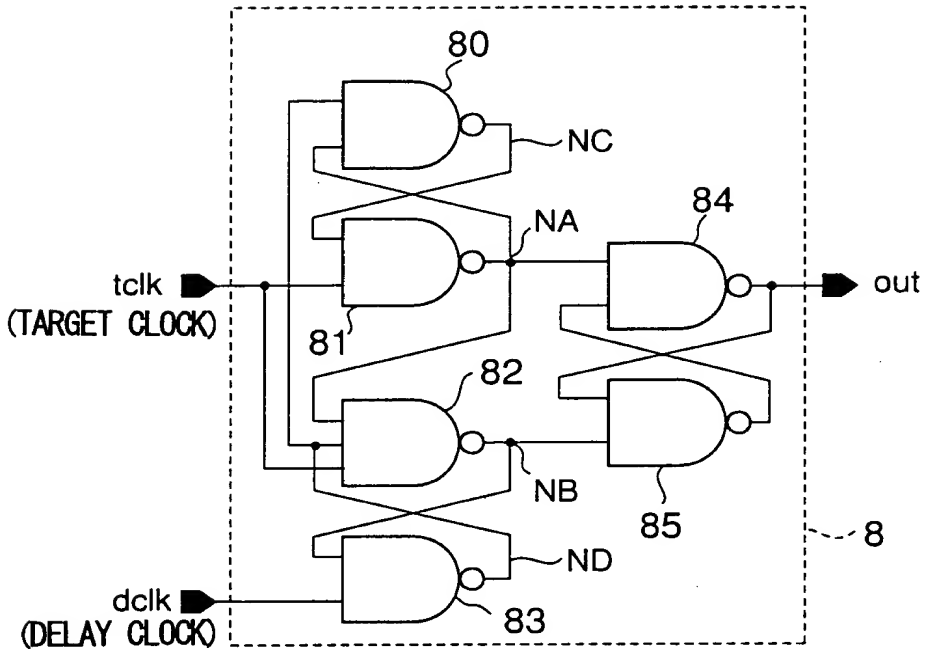

80
NC
84
NA
tclk
(TARGET CLOCK)
out
81
82
NB
85
8
ND
dclk
(DELAY CLOCK)
83

FIG. 9

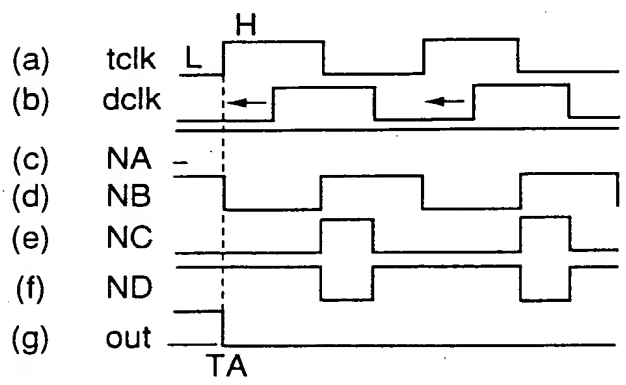

H
(a) tclk
L
(b) dclk
(c) NA
(d) NB
(e) NC
(f) ND
(g) out
TA

FIG. 10

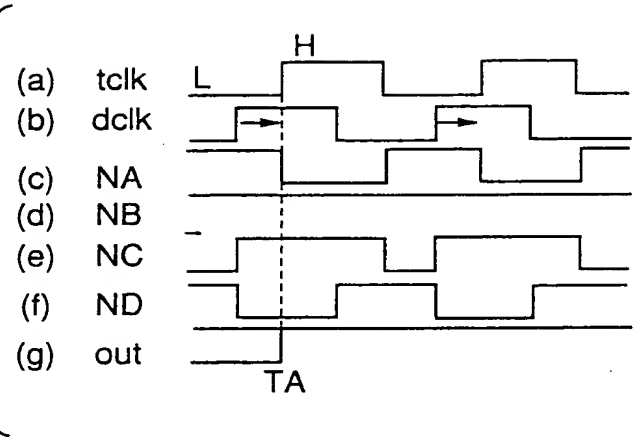
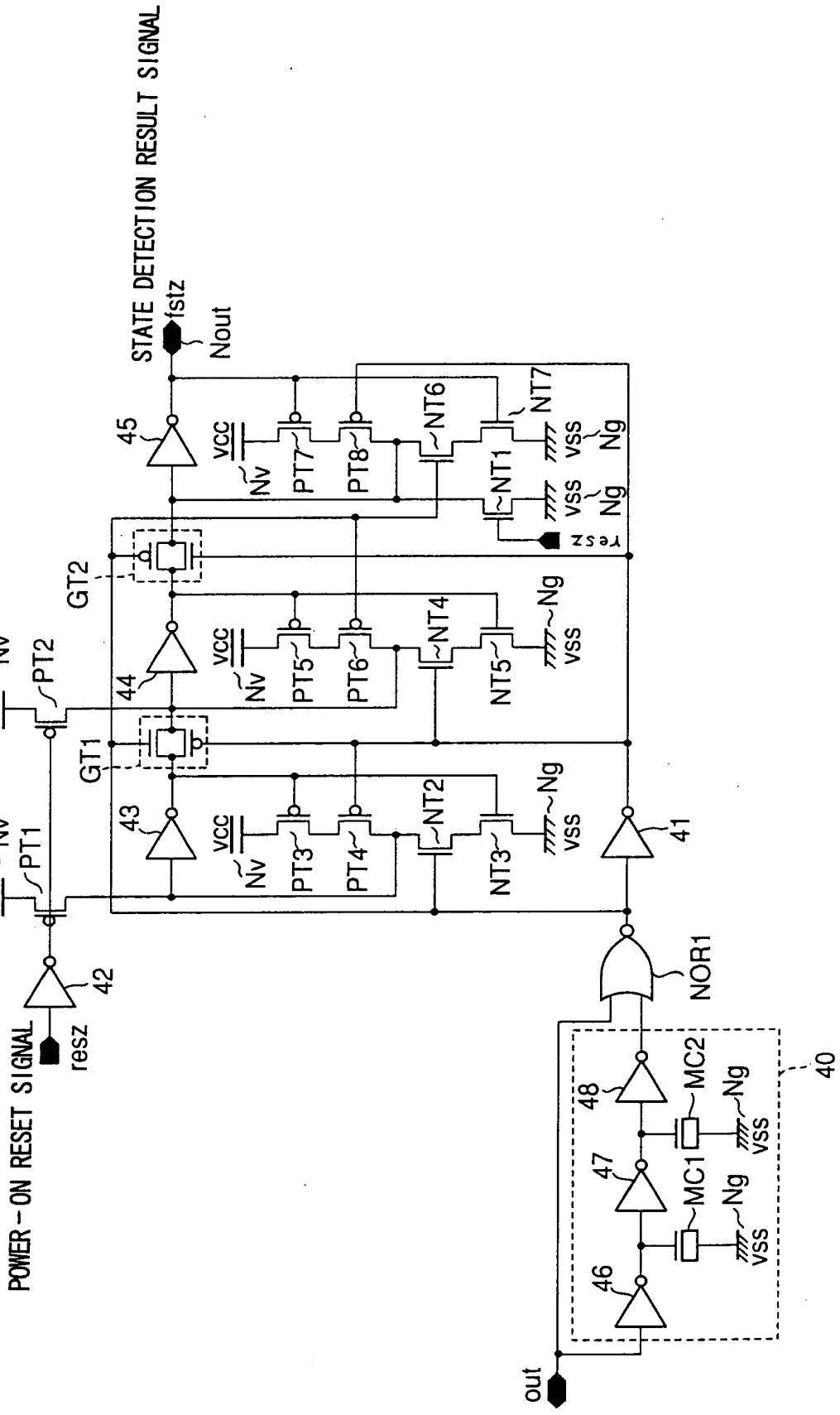


FIG. 11


STATE DETECTION RESULT SIGNAL
fstz
Nout
POWER-ON RESET SIGNAL
resz
out
NOR1
GT1
GT2
vcc
Nv
Ng
vss
resz
PT1
PT2
PT3
PT4
PT5
PT6
PT7
PT8
NT1
NT2
NT3
NT4
NT5
NT6
NT7
MC1
MC2
40
41
42
43
44
45
46
47
48

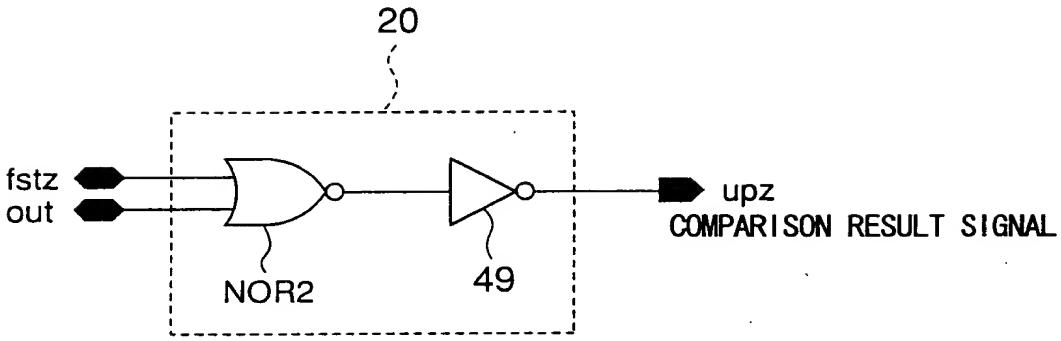



FIG. 12